REMARKS

Claims 1-3 are pending. The Examiner sustained his objections to the drawings and specification, along with his rejections of the claims. Each of these objections and rejections have been obviated by argument and/or amendment as described in the following sections. Accordingly, Applicant respectfully requests that the Examiner withdraw the objections and rejections and issue a Notice of Allowance for claims 1-3 and 6.

A. Drawing Objections

The Examiner sustains the objection to the drawings as not showing every claimed feature pursuant to 37 CFR 1.83(a). IN particular, the Examiner objects to a "solder-containing compound" not being shown. In response to this objection, Applicant has submitted a proposed drawing change to add Fig. 12, which is a flow diagram that discloses a method for making an integrated circuit stack module according to one embodiment of the invention. The flow diagram of Fig. 12, among other things, recites the act of applying a solder-containing compound to a plurality of members, at steps 62 and 65. Thus, it shows an embodiment of the claimed "solder-containing compound application step. Claims 1 through 3 and 6 are process (or method) claims. As such, FIG. 12 satisfies the requirement under Rule 1.83(a) pursuant to Rule 1.81(b), which states that, "drawings may include illustrations which facilitate an understanding of the invention (for example, flow-sheets in cases of processes, and diagrammatic views)." Accordingly, it is urged that the drawing objection be withdrawn.

B. Specification Objections

The Examiner objects to the specification because it is not clear that it provides antecedent basis for the claim term: "plural iterations." To expedite prosecution, in response to this objection, Applicant has amended the claims to remove this term. In particular, claim 2 has

been amended to recite "in which the carrier frame is provided from a carrier bed having a plurality of carrier frames" rather than "in which plural iterations of the carrier frame are created in a carrier bed." This change is fully supported by Fig. 11 and the accompanying description in the specification. Thus, it is urged that this objection be withdrawn.

C. Section 112 Claim Rejections

The Examiner rejected claims 1-3 as being indefinite under 35 U.S.C. 112, second paragraph. Claim 1 is rejected because it is unclear whether the term, "solder-containing compound" as recited in the second and fifth steps are the same. In response to this rejection, Applicant has amended claim 1 to now recite: "applying a first portion of a solder-containing compound . . ." and "applying a second portion of a solder-containing compound . . ." This should make it clear that separate portions of a solder-containing compound are applied to the first and second sides of the plurality of members.

Similarly, the Examiner found the use of the term: "solder connections" in both the third and sixth steps to be unclear as to whether or not they are the same. In response to this rejection, Applicant has amended claim 1 to recite "a first set of solder connections . . ." in the third claim step and "a second set of solder connections . . ." in the sixth claim step to clarify that they are not the same connections.

Finally, the Examiner found the term "plural iterations" in claim 2 to be relative and unclear. As noted above with regard to the specification objection, Applicant has removed this term from the claims. Thus, the claims are now clear pursuant to the second paragraph of Section 112, and it is requested that the rejections be withdrawn.

D. Section 103 Claim Rejections

The Examiner sustained his rejections of claims 1-3 as being obvious over Hikita (U.S. Pat. No. 6,133,637) in view of Sakai (U.S. Pat. No. 5,894,984). The Examiner points out that Hikita teaches (at Figs. 43-45 and accompanying description) placing integrated circuits (14, 16) with leads (14A, 16A) that have solder containing compound (14C, 16B) on contact members; and processing the packaged integrated circuits and the carrier frame using transfer molding to make solder connections between the integrated circuits and the contact members. From this, the Examiner contends that Hikita teaches the claimed method of claim 1 except that it doesn't directly teach processing the IC and frame members by heating them. Therefore, Sakai is presented to fill this gap as it teaches the act of using heat in a transfer molding step. The Examiner thereby asserts that Hikita and Sakai disclose Applicant's claimed method of making a stacked module of packaged integrated circuit devices (hereinafter, "ICs"). Applicant traverses this rejection because in fact, Hikita and Sakai—either alone or in combination—do not teach Applicant's claimed method.

Unlike Applicants' method as recited in amended claim 1, Hikita teaches sandwiching, at the same time in one basic step, the upper and lower ICs (14, 16) together about the frame contacts (12b) at their pads (14A, 16A). With the pads being provided with solder bumps (14C, 16B), electrical solder connections are formed between the electrode pads and lead frame members when the two ICs are compressed together. (See Hikita, col. 21, ll. 3-21). In contrast, Applicants' claim 1 recites applying the first portion of a solder containing compound, then applying the first IC and heating it to form the solder connections between the first IC and contact members. After this is done, the same steps are implemented for separately applying the

second IC. Therefore, the cited art does not make obvious amended claim 1 along with its dependant claims 2 and 3.

New claim 6 is also patentably distinct over the cited art but for separate reasons. New claim 6 recites that the first and second ICs are "packaged" with "external leads extending away from the packaged integrated circuit." Thus, claim 6 recites an embodiment with ICs that are already packaged and have external, extending away, leads, rather than the internal, electrode pad leads taught by Hikita. This is evidenced by the fact that Hikita teaches using transfer molding to package the assembly with an epoxy or resin after both "naked" ICs are connected to the lead frame. (That is, the Hikita ICs are not "packaged when they are connected to the lead frame 12.) This is consistent with the ordinary meaning of "packaged," which in one published technical glossary, is defined as follows:

> The protective container or housing for an electronic component or die, with external terminals to provide electrical access to the components inside.

(See Intersil's Glossary of Semiconductor Terms at http://rel.intersil.com/docs/lexicon/P.html). From this definition, Hikita's ICs (14, 16) are clearly not packaged until the entire module is "packaged" in a resin or epoxy through transfer molding with the lead frame leads (12b) providing connectivity to the interior ICs. This "packaged" limitation is not unimportant. Applicant's inventive method allows for off-the-shelf, packaged ICs, old or new, to be stacked in a reliable, effective manner. Moreover, Hikita clearly does not disclose IC leads that extend away from the IC. It instead teaches electrode pad leads contained within the footprint of the IC die. Thus, the cited art does not make obvious new claim 6 and it too should be allowed.

CONCLUSION

Applicant believes the claims to be patentable over the cited prior art. Accordingly, a Notice of Allowance is respectfully requested. If the Examiner has any questions or concerns whatsoever, he is encouraged to immediately contact Erik Nordstrom at 512/238-7253.

via facsimile

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